P-Channel 150-V (D-S) MOSFET

Key Features:

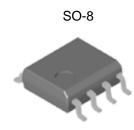
- Low r_{DS(on)} trench technology
- · Low thermal impedance
- Fast switching speed

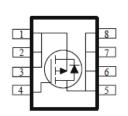
Typical	Дþ	plica	atior	ıs:
.,	, .P		~	

- White LED boost converters
- · Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)}(m\Omega)$	I□ (A)	
-150	260 @ V _{GS} = -10V	-2.9	
	280 @ V _{GS} = -5.5V	-2.8	







ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter			Limit	Units	
Drain-Source Voltage		V_{DS}	-150	V	
Gate-Source Voltage	V_{GS}	±20	V		
Continuous Drain Current ^a $ \frac{T_A=25}{T_A=70} $		· I _D	-2.9		
		'D	-2.4	Α	
Pulsed Drain Current ^b	I _{DM}	-12			
Continuous Source Current (Diode Conduction) a	I _S	-3	Α		
Power Dissipation ^a	T _A =25°C	P_{D}	3.1	W	
T _A =70°C		' D	2.2	VV	
Operating Junction and Storage Temperature Range			-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter			Maximum	Units	
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	40	°C/W	
Maximum Junction-to-Ambient	Steady State	IXOJA	80	C/VV	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Electrical Characteristics

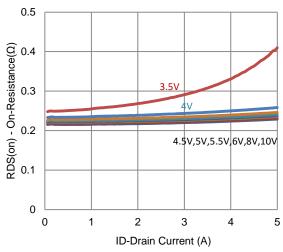
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \text{ uA}$	-1			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±10	uA	
Zero Gate Voltage Drain Current	1	$V_{DS} = -120 \text{ V}, V_{GS} = 0 \text{ V}$			-1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -120 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$		-10	uA		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-4			Α	
Dunin Course On Braintana a	r	$V_{GS} = -10 \text{ V}, I_{D} = -2 \text{ A}$			260	0	
Drain-Source On-Resistance ^a	r _{DS(on)}	$V_{GS} = -5.5 \text{ V}, I_D = -1.6 \text{ A}$			280	mΩ	
Forward Transconductance a	g _{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -2 \text{ A}$		7		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.5 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8		V	
		Dynamic ^b					
Total Gate Charge	Q_g	$V_{DS} = -75 \text{ V}, V_{GS} = -5.5 \text{ V},$		21			
Gate-Source Charge	Q_{gs}	$I_{D} = -2 \text{ A}$		5.8		nC	
Gate-Drain Charge	Q_{gd}	10 - 2 A		8.1			
Turn-On Delay Time	t _{d(on)}	$V_{DS} = -75 \text{ V}, R_{L} = 37.5 \Omega,$		8			
Rise Time	t _r	$V_{DS} = -75 \text{ V}, K_L - 37.3 \Omega,$ $I_D = -2 \text{ A},$		20		no	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = -10 \text{ V}, R_{GEN} = 6 \Omega$		115		ns	
Fall Time	t_f	VGEN = 10 V, NGEN = 0 12		135			
Input Capacitance	C _{iss}			1944			
Output Capacitance	C _{oss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$	_	177	_	рF	
Reverse Transfer Capacitance	C _{rss}			112	_		

Notes

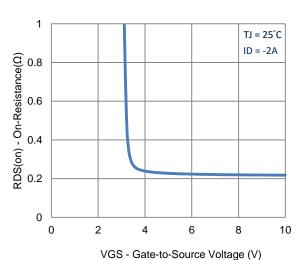
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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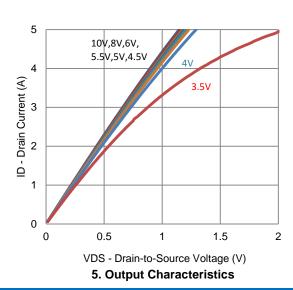
Typical Electrical Characteristics

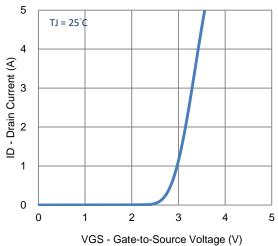


1. On-Resistance vs. Drain Current

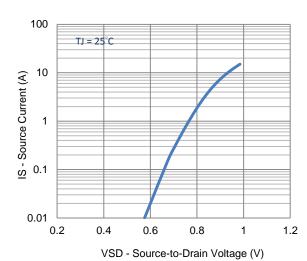


3. On-Resistance vs. Gate-to-Source Voltage

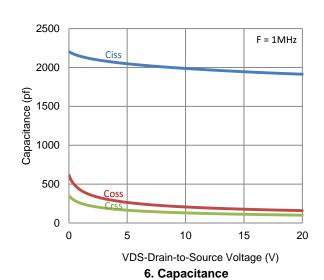




2. Transfer Characteristics

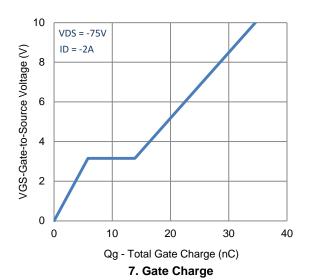


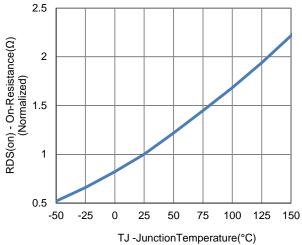
4. Drain-to-Source Forward Voltage

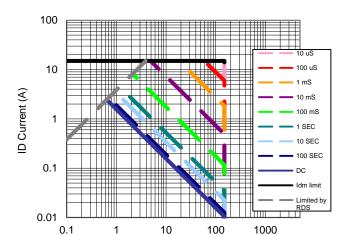


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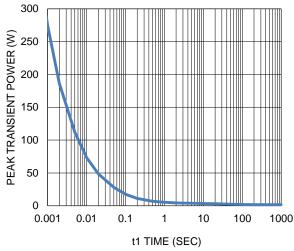
Typical Electrical Characteristics







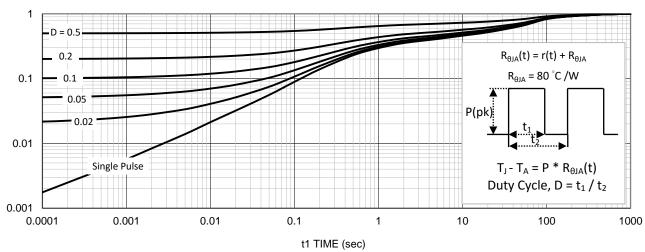
8. Normalized On-Resistance Vs Junction Temperature



VDS Drain to Source Voltage (V)

9. Safe Operating Area

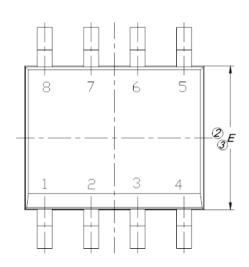
10. Single Pulse Maximum Power Dissipation

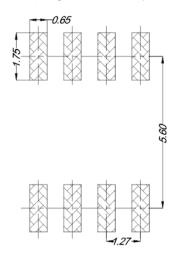


11. Normalized Thermal Transient Junction to Ambient

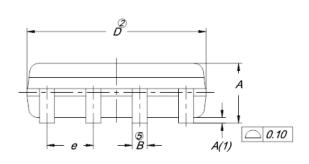
Package Information

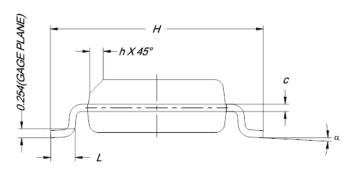
Land Pattern (Only for Reference)





5114	MILLIMETERS				
DIM.	MIN. NOM.		MAX.		
Α	1.35	1.55	1.75		
A(1)	0.10	0.18	0.25		
В	0.38	0.45	0.51		
С	0.19	0.22	0.25		
D	4.80	4.90	5.00		
E	3.80	3.90	4.00		
е	1.27 BSC				
Н	5.80	6.00	6.20		
L	0.50	0.72	0.93		
α	0°	4°	8°		
h	0.25	0.38	0.50		





Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.